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1 Fast functional simulation using branching programs

Pranav Ashar, Sharad Malik

December 1995 **Proceedings of the 1995 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(97.71 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Abstract: This paper addresses the problem of speeding up functional (delay-independent) logic simulation for synchronous digital systems. The problem needs very little new motivation-cycle-based functional simulation is the largest consumer of computing cycles in system design. Most existing simulators for this task can he classified as being either event driven or levelized compiled-code, with the levelized compiled code simulators generally being considered faster for this task. An alternativ ...

Keywords: Boolean functions, benchmark circuits, branching programs, circuit analysis computing, compiled code simulation, cycle-based functional simulation, decision theory, fast functional simulation, functional delay-independent logic simulation, levelized compiled-code, logic CAD, logic design, switch level functional simulation, synchronous digital systems, system design

2 Automated Modeling of Custom Digital Circuits for Test

S. Bose

March 2002 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(156.90 KB) Publisher Site Additional Information: full citation, abstract

Models meant for logic verification and simulation areoften used for ATPG. For custom digital circuits, these modelscontain many tristate devices, which leads to lower faultcoverage. Unlike other research in the literature, the modelingalgorithms presented in this paper analyze each channelconnected component in the context of its environment,thereby capturing the relationship among its input signals.This reduces the number of tristates and increases the modelingefficiency, as measured by fault ...

3 Power analysis of a 32-bit RISC microcontroller integrated with a 16-bit DSP
R. S. Bajwa, N. Schumann, H. Kojima
August 1997 **Proceedings of the 1997 international symposium on Low power electronics and design**
Full text available: pdf(727.17 KB) Additional Information: full citation, references, citings

4 Design aids and hardware testing of microprocessor system circuit packs
J. Grason
February 1977 **Proceedings of the Symposium on Design Automation and Microprocessors**
Full text available: pdf(444.58 KB) Additional Information: full citation, abstract, references, index terms

In this paper the hardware testing of microprocessor system circuit packs is treated, with particular emphasis on the role of automatic design aids in this process. Specific problems of implementing these tests on automatic test machines are also considered. Goals and methods of testing in this context are discussed, with special attention paid to functional simulation as a design aid. Several unique problems this type of testing are discussed, including tri-state busses, dynamic RAMs, PROM ...

5 SSIM: a software levelized compiled-code simulator
L.-T. Wang, N. E. Hoover, E. H. Porter, J. J. Zasio
October 1987 **24th ACM/IEEE conference proceedings on Design automation conference**
Full text available: pdf(765.27 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents a new logic simulation technique that uses software levelized compiled-code (LCC) for synchronous designs. Three approaches are proposed: C source code, target machine code and interpreted code. The evaluation speed for the software LCC simulator (SSIM) is about 140,000 (gate) evaluations per second using C source code or target machine code, or 50,000 evaluations per second using interpreted code. It is about 40 to 100 times slower than the AIDA hardware LCC simulator, ...

6 On removing redundancy in sequential circuits
Kwang-Ting Cheng
June 1991 **Proceedings of the 28th conference on ACM/IEEE design automation conference**
Full text available: pdf(747.28 KB) Additional Information: full citation, references, citings, index terms

7 Contest: a concurrent test generator for sequential circuits
Vishwani D. Agrawal, Kwang-Ting Cheng, Prathima Agrawal
June 1988 **Proceedings of the 25th ACM/IEEE conference on Design automation**
Full text available: pdf(764.79 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes the application of a concurrent fault simulator to automatic test vector generation. As faults are simulated in the fault simulator a cost function is simultaneously computed. A simple cost function is the distance (in terms of the number of gates and flip-flops) of a fault effect from a primary output. The input vector is then modified to reduce the cost function until a test is found. The paper presents experimental results showing the effectiveness of this method in ...

8 ClariNet: a noise analysis tool for deep submicron design

Rafi Levy, David Blaauw, Gabi Braca, Aurobindo Dasgupta, Amir Grinshpon, Chanlee Oh, Boaz Orshav, Supamas Sirichotiyakul, Vladimir Zolotov

June 2000 **Proceedings of the 37th conference on Design automation**

Full text available: pdf(101.67 KB) Additional Information: full citation, abstract, references, citings, index terms

Coupled noise analysis has become a critical issue for deep-submicron, high performance design. In this paper, we present, ClariNet, an industrial noise analysis tool, which was developed to efficiently analyze large, high performance processor designs. We present the overall approach and tool flow of ClariNet and discuss three critical large-processor design issues which have received limited discussion in the past. First, we present how the driver gates of a coupled interconnect network a ...

9 Gate-level test generation for sequential circuits

Kwang-Ting Cheng

October 1996 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 1 Issue 4

Full text available: pdf(448.19 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper discusses the gate-level automatic test pattern generation (ATPG) methods and techniques for sequential circuits. The basic concepts, examples, advantages, and limitations of representative methods are reviewed in detail. The relationship between gate-level sequential circuit ATPG and the partial scan design is also discussed.

Keywords: IC testing, automatic test generation, sequential circuit test generation, testing

10 Digital test generation and design for testability

John Grason, Andrew W. Nagle

June 1980 **Proceedings of the seventeenth design automation conference on Design automation**

Full text available: pdf(1.42 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper is a tutorial intended primarily for individuals just getting started in digital testing. Basic concepts of testing are described, and the steps in the test development process are discussed. A pragmatic approach to test sequence generation is presented, oriented towards ICs interconnected on a board. Finally, design for testability techniques are described, with an emphasis on solving problems that appeared during the test generation discussion.

11 Test generation for MOS circuits using D-algorithm

Sunil K. Jain, Vishwani D. Agrawal

June 1983 **Proceedings of the twentieth design automation conference on Design automation**

Full text available: pdf(570.05 KB) Additional Information: full citation, abstract, references, citings, index terms

An application of the D-algorithm in generating tests for MOS circuit faults is described. The MOS circuits considered are combinational and acyclic but may contain transmission gates and buses. Tests are generated for both, the stuck type faults and the transistor faults (open and short). A logic model is derived for the MOS circuits. In addition to the conventional logic gates, a new type of modeling block is used to represent the "memory" state caused by the "ope ...

12 Power minimization in IC design: principles and applications

Massoud Pedram

January 1996 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 1 Issue 1

Full text available: pdf(550.02 KB) Additional Information: full citation, abstract, references, citings, index terms

Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift in which power dissipation is as important as performance and area. This article presents an in-depth survey of CAD methodologies and techniques for designing low power digital CMOS circuits and systems and describes the many issues facing designers at architectural, logical, and physical levels of design abstraction. It reviews some of the techniques and tool ...

Keywords: CMOS circuits, adiabatic circuits, computer-aided design of VLSI, dynamic power dissipation, energy-delay product, gated clocks, layout, low power layout, low power synthesis, lower-power design, power analysis and estimation, power management, power minimization and management, probabilistic analysis, silicon-on-insulator technology, statistical sampling, switched capacitance, switching activity, symbolic simulation, synthesis, system design

13 Acceleration techniques for dynamic vector compaction

Anand Raghunathan, Srimat T. Chakradhar

December 1995 **Proceedings of the 1995 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(176.26 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

We present several techniques for accelerating dynamic vector compaction for combinational and sequential circuits. A key feature of all our techniques is that they significantly improve the computation times without adversely affecting the quality of test sets that can be derived using state-of-the-art compaction methods. Our techniques are based on three key ideas: (1) identification of support sets, (2) target fault switching, and (3) use of dynamic equivalent and untestable fault analysis. A ...

Keywords: Acceleration Techniques, Dynamic equivalent and untestable fault analysis, Target fault switching, Test compaction, Support sets

14 A hybrid numeric/symbolic program for checking functional and timing compatibility of synthesized designs

Chih Tung Chen, Alice C. Parker

May 1984 **Proceedings of the 7th international symposium on High-level synthesis**

Full text available: pdf(588.17 KB) Additional Information: full citation, references

15 High-level design verification of microprocessors via error modeling

D. Van Campenhout, H. Al-Asaad, J. P. Hayes, T. Mudge, R. B. Brown

October 1998 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 3 Issue 4

Full text available: pdf(174.30 KB) Additional Information: full citation, abstract, references, citings, index terms

A design verification methodology for microprocessor hardware based on modeling design errors and generating simulation vectors for the modeled errors via physical fault testing techniques is presented. We have systematically collected design error data from a number of microprocessor design projects. The error data is used to derive error models suitable for design verification testing. A class of basic error models is identified and shown to yield tests that provide good coverage of comm ...

Keywords: design errors, design verification, error modeling

16 Static compaction using overlapped restoration and segment pruning

Surendra K. Bommu, Srimat T. Chakradhar, Kiran B. Doreswamy

November 1998 **Proceedings of the 1998 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(854.22 KB) Additional Information: full citation, references, citings, index terms

17 Automated multi-cycle symbolic timing verification of microprocessor-based designs

Anurag P. Gupta, Daniel P. Siewiorek

June 1994 **Proceedings of the 31st annual conference on Design automation conference**

Full text available: pdf(140.84 KB) Additional Information: full citation, references, citings, index terms

18 Functional verification of MOS circuits

D. Weise

October 1987 **24th ACM/IEEE conference proceedings on Design automation conference**

Full text available: pdf(697.85 KB) Additional Information: full citation, abstract, references, citings, index terms

This report describes the ideas behind Silica Pithecus, a program which verifies synchronous digital MOS VLSI circuits. Silica Pithecus accepts the schematic of an MOS VLSI circuit, declarations of the logical relationships between the inputs signals (e.g., which inputs are mutually exclusive), and a specification of the intended digital behavior of the circuit. If the circuit fails to meet its specification Silica Pithecus returns to the designer the precise reason it fail ...

19 Verischemelog: Verilog embedded in Scheme

James Jennings, Eric Beuscher

December 1999 **ACM SIGPLAN Notices , Proceedings of the 2nd conference on Domain-specific languages**, Volume 35 Issue 1

Full text available: pdf(760.35 KB) Additional Information: full citation, abstract, references, index terms

Verischemelog (pronounced with 5 syllables, veruh-scheme-uh-log) is a language and programming environment embedded in Scheme for designing digital electronic hardware systems and for controlling the simulation of these circuits. Simulation is performed by a separate program, often a commercial product. Verischemelog compiles to Verilog, an industry standard language accepted by several commercial and public domain simulators.Because many ...

20 Automatic generation of assertions for formal verification of PowerPC microprocessor arrays using symbolic trajectory evaluation

Li-C. Wang, Magdy S. Abadir, Nari Krishnamurthy

May 1998 **Proceedings of the 35th annual conference on Design automation conference**

Full text available: pdf(212.91 KB) Additional Information: full citation, abstract, references, index terms

For verifying complex sequen tialbloc ks such as microprocessor embedded arrays, the formal method of symbolic trajectory ev aluation (STE) has achieved great success in the past [[3], [5], [6]]. P ast STE methodology for arrays requires manual creation of "assertions" to which both the RTL view and the actual design should be equivalent. In this paper, w e describe a novel method to automate the assertion creation process which improves the efficiency and the quality of array v ...

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